CURRICULAM VIATE

Dr. Saurabh Sharma

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Mob. 8958838155,9536017773
GE-27,Global city GanganagarMeerut

OBJECTIVE

Seeking a position to utilize my skills and abilities while being resourceful, innovative and flexible. As Academicians, I am creative and striving for excellence so as to secure a challenging position which will enable me to integrate my knowledge and skills.

WORK/TEACHING/ADMINISTRATIVEEXPERIENCE (16 YEARS)

- **Working as a Director (IQAC)** , Amrapali Group of institution (Haldwani) Uttrakhand (From December 2022 to Till now)
- Worked As Dean (Academic, Admission & Administration) in Shanti Niketan Group Of Institution , Meerut (Affiliated to CCS University (Meerut)/AKTU & BTE (Lucknow) from October 2018 to December 2022
- Worked as Dean (Academic) & **Associate Professor,** in Department of Electronics and Communication at SITE, Subharti University (Meerut) from July from July 2015 to October 2018
- Worked as **Assistant Professor and Head ,**in Department of Electronics and Communication at **MEERUT INSTITUTE OF ENGINEERING &TECHNOLOGY(MEERUT) from Oct 2010 to June 2015**
- **Worked as a Design Engineer in Acctel Technology, Singapore as an ASIC Design Engineer since June 2010 to Oct 2010.**
- Had teaching Assistant ship in EC dept.at **N.I.T. Hamirpur**(H.P.) from **Aug 2008 to May 2010**.
- Worked as a Lecturer in Department Of Electronics & Communication at **College Of Engineering & RuralTechnology from July 2007- july 2008.**

EUCATIONAL QUALIFICATION

- **Ph.D. In VLSI & Embedded System From Swami Vivekanand Subharti University , (Meerut) (2019-2022)**
- **MBA from Himalayan Garhwal University (Uttrakhand) 2017-2019**
- **M.Tech.** In VLSI (**7.19 CGPI**) from **National Institute Of Technology(NIT),Hamirpr (HP)**. Year of passing **July 2010**.
- **B.Tech.** in Electronics and Communication Engineering (**65%**) from **UPTU Lucknow** (U.P.)Year of passing: **July2006**.
- **12**th from U.P. Board**,(66.4%) Govt. inter College** Bijnor (U.P.)**June2000**
- **10**th from U.P.Board**, (70.3%) Govt. higher secondary School** Pati Pithoragarh (Uttarakhand) **June 1998.**

GATE & UPPCS RESULTS

- **Qualified UPPCS 2018 & 2019 Prelims**
- **Qualified GATE in 2008 with 97.2 percentile.**
- **Qualified GATE in2009 with 98.8 percentile.**

ADMINISTRATIVE POSITIONS

1. Worked as Dean Academic And administration in SNGI Meerut
2. Worked as Head Of The department during the year 2010-2015 in Meerut Institute Of Technology, Meerut
3. In charge Of Mission10X MTLC center in Meerut Institute Of Technology.
4. Member of planning board in Meerut institute of technology.

RESEARCH EXPERIENCE AND GATECLASSES

- **Published more than10 research paper with the students i n reputed journal / Conference by their project.**
- **Taught in Gate classes in Gate study Center at MIT,Meerut**

PUBLICATIONS

I. National Conferences

1. SaurabhSharma,MonikaSingh,AshwaniRana"MoscurrentmodeLogicinSubThreshold Region" Published in proceeding RAEEE-09 PP. 430-434
2. SaurabhSharma,MonikaSingh,Dr.RajooPandey"AnalysisoftheWavelengthPropagation for Free Space Optical Communication" Published in proceeding RAEEE-09 pp.420-424
3. Saurabh Sharma, Sunil Jadav, Gaurav Saini, Manoj Kumar "Low Power Track-and-Hold Circuit for Wideband Acquisition System in 0.18um CMOS Technology" Published in "NCWCVD-2010"march27-28,2010,NationalConferenceonWirelessCommunication& VLSI Design, Gwalior Engineering College, Gwalior (M.P)
4. Saurabh Sharma, Gaurav Saini, Sunil Jadav, Saurabh Sharma "Carbon Nanotubes & its Application for VLSI Interconnects in Wireless Comm." ,Published in "E-Manthan-2010" April 02-03 ,2010 ,National Conference on Electronics Comm. & Instrumentation Collaboration with IETE, College of Science & Engineering, Jhansi (U.P), pp.159-162
5. Saurabh Sharma, Manoj Bansal "Comparison of Static and Dynamic CMOS Logic" publishedinproceedingTSPC-2011,NationalconferenceonTrendsinSignalProcessingand Communication (10-12 March-2011) at Bhagwant institute of technology Muzaffarnagar (U.P.)

II. InternationalConferences

1. SaurabhSharma,AshwaniRana"OptimizationofMCMLunitcellin100nmtechnology" published in International conference of computer and communication ICCCE 2011 NIT Hamirpur.
2. SaurabhSharma,AshwaniRana "Performanceoptimization ofMOS current modelogic in 100nmtechnology"organizedbydepartmentofcomputerscienceBanarasHinduuniversity (BHU)

III. International Journals :

1. Saurabh Sharma, Ashwani Rana "A new approach of LowPowerMCML"international journal of Engineering and technology (IJET) DEC 2011

2. Saurabh Sharma, Ashutosh bhardwaj, Sanjeev Maheshwari, "Elimination of Charge sharing Problem in Dynamic Circuits"published in IJECCE volume no.4 issue on 2 April 2013

3. SaurabhsharmaAshwaniRana,"OptimizationandPerformenceEvaluationOfMosCurrent Mode Logic in 35 nm" International Journal of Scientific & Engineering Research (IJSER) -(ISSN2229-5518)onOctober2011(Volume4,Issue9,August 13)

4. Sanjeev Maheshwari , Saurabh Sharma, Madhuri Garg, Rohit Agarwal, Vishal Singh "Exploiting TheBody Of MOS Devices for highperformance analog Design"publishedin IJARCCE volume no. 3 issue 2 Feb 2014

5. Saurabh Sharma, Ashutosh Bhardwaj,Sanjeev Maheshwari "Reduction of Leakage Current in Domino Logic using Bulk terminal of MOS" published in International conference of Recent technology in Advance Electronics (11-12 April 2013)-PP-10

6. SaurabhSharma,VashuSharma,Urvashi Chaudhary,JaiVyas"Power-GatedMOSCurrent Mode Logic (PG-MCML) technique used to decrease the power delay product of MCML2 issue 3 March 2014

7. Saurabh Sharma,Vashu Sharma,Urvashi Chaudhary,Jai Vyas"Power-Gated MOS Current Mode Logic (PG-MCML) technique used to decrease the power delay product of MCML 2 issue 3 March 2014

9. Sanjeev Maheshwari ,Saurabh Sharma,Madhuri Garg,Rohit Agarwal, Vishal Singh "Comparitive Study Of Single Gate,Soi And Double GateMosfet"publishedin IJARCCE volume no. 3 issue 2 feb 2014

10. Sanjeev Maheshwari ,Saurabh Sharma, Madhuri Garg,Rohit Agarwal, Vishal Singh "Improvement of Linearity of Analog Amplifier with Gain Booster Circuit " published in IJARCCE volume no. 4 issue 2 march 2014

WORKSHOPANDSEMINAR

1. Attended Two days workshop on "**Research issues in modern VLSI devices**" (RIMVD- 09) from November 06-07, 2009 organized by Department of Electronics and communication Engineering ,N.I.T. Hamirpur(H.P.)

2. Attendedonedayworkshopon"**UsagesofE-Resources**"organizedbycentrallibrary N.I.T.Hamirpur (H.P)heldon9thAug2008

3. Attended 2 days workshop on "Emerging **Research areas in VLSI and communication**"(ERA)20-21may2010organized by Department of Electronics and communication Engineering ,N.I.T. Hamirpur(H.P.)

4. Workshop on Embedded system Under Wipro Mission 10X @ Wipro Tech Bangalore (24-28 June 2013)

5. Workshop on advance Embedded system Under Wipro Mission10X@WiproTech Bangalore (27-29 October 2013)

6. AICTE Recognized Short Term Course On Computer Network Using CCNA Through ICT @ NITTTR Chandigarh (10-14 Mar 2014)

AREAOF INTEREST

- ELECTRONIC CIRCUIT
- SEMICONDUCTOR DEVICE
- VLSI DESIGN
- DIGITAL DESIGN

MEMBERSHIP

1. **Memberof IEEE**
2. **Memberof ISTE**

TOOLSKNOWN

- **EDA Simulation tool:** T-SPICE,H-SPICE,MENTORGRAPHICS,TCAD-SILVACO

MINIPROJECT

7. **Project title:** "**Temperature independency of MOS Current Mode logic in Sub Threshold Region**"

TOOL: TANNEREDA,H-SPICE

SUPERVISOR: Dr.AshwaniRana

MAJORPROJECT(DISSERTATION)

Project title : **MOS CURRENT MODE LOGIC-Analysis and design**

TOOL:TANNER EDA,H-SPICE

SUPERVISOR: Dr.AshwaniRana

STRENGTH&ABILITIES

1. Good analytical skills
2. Hardworking
3. Adaptability
4. Positive approach towards problems
5. Positive attitude
6. Strong Determination
7. Decision making ability and confidence
8. Communication skills
9. Integrity and ready to accept challenges
10. Result oriented

Extra-CurriculaRACTIVITIES

1. Organized National conference **RAEEE-09** @N.I.T.Hamirpur.
2. Organized workshop **(RIMVD-09)** in ECdeptt. @ N.I.T.Hamirpur.
3. Held the responsibility to organizeTECH-FESTof thecollege.

PERSONALEINFORMATION

Name	Saurabh Sharma
Father's Name	Vinod kumar Sharma
Gender	Male
Date of birth	5thAUG1984
Nationality	Indian
Language known	Hindi,English

CONTACTINFORMATION

PermanentAddress	Pragati Vihar colony lane no.2nd Bijnor (U.P.)-246701
PresentAddress	Pragati vihar colony lane no.2ndBijnor(U.P.)-246701
CellPhone:	+918958838155,9536017773
e-Mail:	sharma.saurabh2006@gmail.com

DECLARATION

I am declaring that all information's given above are correct in best of my knowledge.

PLACE: MEERUT **(SAURABH SHARMA)**
DATE: