Printed Pages : 4 EEC302

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0323 Roll No.

B.Tech

(SEM III) ODD SEMESTER THEORY EXAMINATION 2009-10

DIGITAL ELECTRONICS

Time : 3 Hours] *[Total Marks : 100*

Note : *Attempt* ***all*** *questions. Each question carries* ***equal*** *marks.*

1 Attempt any **four** parts :

(a) Explain the signed binary number representation.

(b) Given the $8-bit$ data word 01011011, generate the 13-bit composite word for the Hamming code that corrects single errors and detects double errors.

(c) Simplify the boolean function in (i) SOP (ii) POS

$$F(x, y, z) = \sum (2, 3, 6, 7)$$

(d) Simplify the following expression and implement it with two-level NAND gate circuit :

$$Y = BD + BC\bar{D} + A\bar{B}\bar{C}\bar{D}$$

(e) Simplify the Boolean function f together with don't-care condition using Karnaugh map :

$$F(w, x, y, z) = \sum (1, 3, 4, 13, 15)$$

$$d(w, x, y, z) = \sum (2, 5, 6, 7)$$

(f) Minimize the following boolean function by using Quine Mc-Clusky method

$$F(A, B, C, D, E) = \sum(20, 28, 37, 39, 48, 56)$$

2 Attempt any **four** parts :

(a) Design a combinational circuit that adds one to a 4-bit binary number, $A_3A_2A_1A_0$. The circuit can be designed using four half-adders.

(b) Show that a full-subtractor can be constructed with two-half-substractors and an OR-gate.

(c) What do you mean by encoder ? Implement the following functions using 3 : 8 decoder.

$$F_1(A, B, C) = \sum(0, 1, 3, 5, 6)$$

$$F_2(A, B, C) = \sum(0, 2, 4, 7,)$$

(d) Describe the decimal adder and demultiplexer.

(e) What is magnitude comparator ? Design a two-bit comparator using logic gates.

(f) Explain the procedure of binary multiplier.

3 Attempt any **two** parts :

(a) Differentiate between latches and flip-flop. Draw and explain a master-slave J-K flip-flop.

(b) Draw the circuit for converting SR flip flop into D flip flop. Also design a one input and one output sequential circuit using D flip flop for the state diagram shown in **Fig. 3.1**

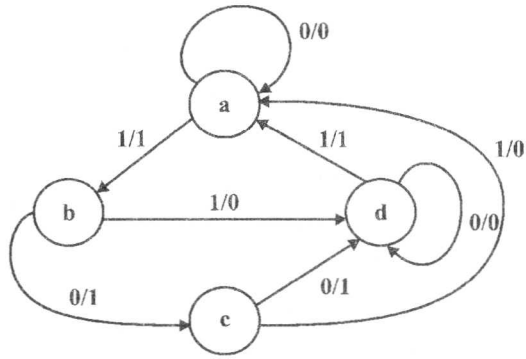

Fig. 3.1

(c) Design a 4-bit binary synchronous counter with D-flip flop. Also briefly describe the universal shift register.

4 Attempt any **two** parts :

(a) Write down the classification of memories. Also draw and explain the programmable logic array.

(b) What is the difference between flow chart and ASM chart ? Also draw an ASM chart and state table for a 2-bit UP-DOWN counter having mode control input :

M=1 : Up counting M = 0. Down counting. The circuit should generate an output 1 whenever count becomes minimum or maximum.

(c) Explain the following :

(i) ROM and PAL

(ii) Realization of ASM chart using multiplexer.

5 Attempt any **two** parts :

(a) Draw the block diagram of asynchronous segmental circuit and explain its working. Also list the different techniques used for state assignment.

(b) An asynchronous sequential circuit has two internal states and one output. The excitation functions and output function of the circuit are as follows :

$$Y_1 = \bar{x}_1 x_2 + x_2 y_1$$

$$Y_2 = x_1 y_2 + x_2$$

Output function

$$Z = x_1 + y_2$$

(i) Derive the logic diagram of the circuit

(ii) Derive the transition table and output map.

(c) Define critical race and non-critical race. What is hazard ? Also explain the elimation of Hazard.