Printed Pages – 4

EEC – 402

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0322 Roll No.

B.Tech.

(SEM IV) EVEN SEMESTER THEORY EXAMINATION, 2009-2010

COMPUTER ARCHITECTURE & ORGANIZATION

Time : 3 Hours *Total Marks : 100*

Note : *(i) Attempt **ALL** the questions.*

*(ii) All questions carry **equal** marks.*

1. Attempt **any four** parts : **(4x5=20)**

(a) What is M/M/1 queueing model of computer system? Explain.

(b) Implement the following functions using PAL.

$W(A,B,C,D) = \Sigma(2,12,13)$

$X(A,B,C,D) = \Sigma(7,8,9,10,11,12,13,14,15)$

$Y(A,B,C,D) = \Sigma(0,2,3,4,5,6,7,8,10,11,15)$

$Z(A,B,C,D) = \Sigma(1,2,8,12,13)$

(c) List various design aspects in the processor level design.

(d) What do you understand by design levels in the design of computer system?

(e) Explain the design process at the register level.

(f) Give the internal structure of a CPU.

2. Attempt **any four** parts : **(4x5=20)**

(a) Write a program to evaluate the arithmetic statement :

$$X = \frac{(A-B) + C*(D*E-F)}{G+H*K}$$

(i) Using an accumulator type computer with one address instructions.

(ii) Using a general register computer with three address instructions.

(b) What are the different instruction formats used in the computer architecture?

(c) What are the major functions of a processor ? Explain them with the help of a flow chart.

(d) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro operation to be performed in order to change the value in A to :

(i) 01101101

(ii) 11111101

(e) Draw and explain the architecture of an accumulator based CPU.

(f) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two address instructions, how many one-address instructions can be formulated?

3. Attempt **any two** parts : **(2x10=20)**

(a) Explain the Booths algorithm for Multiplication. Perform $(+15) \times (-13)$ using Booth algorithm. Assume 5 - bit registers that hold signed numbers.

(b) Draw and explain the flow chart for floating point division.

(c) Draw a space '- time diagram for a six - segment pipeline showing the time it takes to process eight tasks. A nonpipeline system takes 50 ns to process a task. The same task can be processed in a six - segment pipeline with a clock cycle of 10 ns. Determine the speed-up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved ?

4. Attempt **any two** parts : **(2x10=20)**

(a) Draw and explain microinstruction sequencing organization.

(b) Explain the sequence of operations needed to perform following CPU functions :

(i) Storing a word in the memory

(ii) Register transfers

(c) What is microprogramming and microprogrammed control unit?

(e) Explain the design process at the register level.

(f) Give the internal structure of a CPU.

2. Attempt **any four** parts : (4x5=20)

(a) Write a program to evaluate the arithmetic statement :

$$X = \frac{(A-B) + C*(D*E-F)}{G+H*K}$$

(i) Using an accumulator type computer with one address instructions.

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(e) Draw and explain the architecture of an accumulator based CPU.

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5. Attempt **any two** parts : **(2x10=20)**

(a) Draw the functional block diagram of microprocessor 8085 and explain it in brief.

(b) Draw and explain the virtual memory organization.

(c) What are the various Mapping Techniques used in the cache organization?

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